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Joseph Smart
David Grider
Shawn Gibb
Brook Hosse
Jeffrey Shealy
INVENTORS

SURFACE PASSIVATION OF GaN DEVICES IN EPITAXIAL GROWTH CHAMBER

Withrow & Terranova, P.L.L.C.
P.O. Box 1287
Cary, NC 27512
(919) 654-4520

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SURFACE PASSIVATION OF GaN DEVICES IN EPITAXIAL GROWTH CHAMBER

[0001] This application claims the benefit of provisional patent application serial number 60/503,917, filed September 19, 2003, the disclosure of which is hereby incorporated by reference in its entirety.

Field of the Invention

[0002] The present invention relates to surface passivation of a gallium nitride (GaN) epitaxial structures, and more particularly relates to thermally assisted deposition of silicon nitride passivation of the GaN structures while in a GaN growth chamber.

Background of the Invention

[0003] Gallium nitride (GaN) offers substantial opportunity to enhance performance of electronic devices such as high electron mobility transistors (HEMTs) and metal-insulator-semiconductor field effect transistors (MISFETs). Epitaxial growth of GaN structures leads to phenomena associated with surface traps, which degrade performance of electronic devices, on the surface of the GaN structure. The surface traps are open bonding sites, on the surface of the GaN structure caused by an abrupt termination of the GaN crystal structure. The reactions associated with surface traps degrade the performance of electronic devices fabricated using the GaN structure by causing radio frequency (RF) dispersion and current collapse.

[0004] In order to avoid degradation of electronic devices due to the surface traps, a passivation layer may be deposited on the surface of the GaN structure. Generally, the passivation layer is a dielectric material capable of passivating, neutralizing, or filling the surface traps. However, conventional methods of passivating the GaN structure, such as plasma enhanced chemical vapor deposited (PECVD) silicon nitride, occur after the growth of the GaN structure and outside of the growth chamber used to grow the GaN structure. Therefore, the GaN structure is exposed to the atmosphere prior to fabrication of the electronic device. By exposing the GaN structure to the

atmosphere, oxidation may occur on the surface of the GaN structure, thereby decreasing the effectiveness and reproducibility of the ex-situ passivation process. Therefore, there remains a need for a GaN structure having a passivation layer deposited before the GaN structure is removed from the growth chamber.

Summary of the Invention

[0005] The present invention relates to passivation of a gallium nitride (GaN) structures before the GaN structure is removed from an epitaxial growth chamber. The GaN structure includes one or more structural epitaxial layers deposited on a substrate and the passivation layer deposited on the structural epitaxial layers. In general, the passivation layer is a dielectric material deposited on the GaN structure that serves to passivate surface traps on the surface of the structural epitaxial layers. Preferably, the passivation layer is a pyrolitic (thermally assisted) silicon nitride (PSN) passivation layer.

[0006] The GaN structure including the PSN passivation layer may be used to fabricate electrical devices such as a high electron mobility transistor (HEMT) or a metal-insulator-semiconductor field effect transistor (MISFET). For the HEMT, the structural epitaxial layers include a transitional layer, a GaN buffer layer, and an aluminum gallium nitride (AlGaN) Schottky layer. Optionally, the structural epitaxial layers may include a sub-buffer layer between the transitional layer and the GaN buffer layer and/or a GaN termination layer deposited on the AlGaN Schottky layer. The PSN passivation layer is etched in order to form source, gate, and drain contacts. The PSN passivation layer serves to essentially eliminate degradation of the operation of the HEMT due to phenomena such as radio frequency (RF) dispersion and current collapse by passivating the surface traps on the surface of the Schottky layer or the optional GaN termination layer. In a similar fashion, the MISFET may be fabricated from the GaN structure including the PSN passivation layer by forming the gate contact on the PSN passivation layer.

[0007] Those skilled in the art will appreciate the scope of the present invention and realize additional aspects thereof after reading the following

detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0008] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the invention, and together with the description serve to explain the principles of the invention.

[0009] Figure 1 illustrates a gallium nitride (GaN) structure having an in-situ pyrolitic silicon nitride (PSN) passivation layer according to one embodiment of the present invention;

[0010] Figure 2 illustrates a high electron mobility transistor (HEMT) having an in-situ PSN passivation layer according to one embodiment of the present invention; and

[0011] Figure 3 illustrates a metal-insulator-semiconductor field effect transistor (MISFET) having an in-situ PSN passivation layer according to one embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0012] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the invention and illustrate the best mode of practicing the invention. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the invention and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0013] Figure 1 illustrates a gallium nitride (GaN) structure having been passivated before removal from a growth chamber (not shown) according to the present invention. The GaN structure 10 includes a substrate 12, structural epitaxial layers 14, and a (pyrolitic silicon nitride) PSN passivation layer 16. In one embodiment, the PSN passivation layer 16 is a thermally assisted silicon nitride passivation layer. The PSN passivation layer 16 is deposited on the structural epitaxial layers 14 prior to removing the GaN structure 10 from the growth chamber, thereby providing a well controlled

environment for the passivation of the surface of the structural epitaxial layers 14 and avoiding exposure of the surface of the structural epitaxial layers 14 to the atmosphere. As a result of the PSN passivation layer 16, GaN electronic devices fabricated using the GaN structure 10 have improved performance and reliability.

[0014] In general, the PSN passivation layer 16 is a dielectric material that passivates the surface traps on the surface of the structural epitaxial layers 14, where the surface traps are unused bonding sites in the crystalline structure of the structural epitaxial layers 14 caused by the abrupt termination of the structural epitaxial layers 14. Due to the insulating nature of the PSN passivation layer 16, the PSN passivation layer 16 is more dense than traditional passivation layers deposited by Plasma Enhanced Chemical Vapor Deposition (PEVCD), thereby providing improved passivation of the surface traps on the surface of the structural epitaxial layers 14. Further, by being more dense than traditional passivation layers, the PSN passivation layer 16 essentially eliminates occurrences of pin-holes, which are holes extending vertically through a layer that may occur especially in thin deposited layers.

[0015] In addition, the PSN passivation layer 16 may be deposited using pyrolysis, which is a thermally activated process commonly know in the art. In general, the deposition of the PSN passivation layer 16 is a high temperature chemical vapor deposition process. Therefore, the deposition of the PSN passivation layer 16 avoids plasma-induced surface damage that may occur in the traditional PECVD passivation process.

[0016] In the illustrated embodiment, the structural epitaxial layers 14 include a nucleation (transitional) layer 18, an aluminum nitride (AlN) sub-buffer layer 20, a GaN buffer layer 22, an aluminum gallium nitride (AlGaN) Schottky layer 24, and a GaN termination layer 26. Although the AlN sub-buffer 20 and the GaN termination layer 26 are described herein as being part of the GaN structure 10, it is important to note that the AlN sub-buffer layer 20 and the GaN termination layer 26 are optional layers that improve the performance of an electronic device fabricated using the GaN structure 10 and are not necessary for the present invention. The substrate 12 may include various materials including but not limited to sapphire or silicon carbide (SiC). The nucleation layer 18 is preferably an aluminum rich layer

such as but not limited to AlGaN. In addition, the structural epitaxial layers 14 may be grown in the growth chamber by various methods including Organic Metallic Vapor-Phase Epitaxy (OMVPE), Molecular Beam Epitaxy (MBE), Hydride Vapor-Phase Epitaxy (HVPE), and Physical Vapor Deposition (PVD).

[0017] When growing the GaN structure 10, the nucleation layer 18 is deposited on the substrate 12. The nucleation layer 18 operates to correct a lattice mismatch between the AlN sub-buffer layer 20 and the substrate 12. In general, a lattice mismatch is created when spacing between atoms of one layer does not match the spacing between atoms of an adjacent layer. As a result of the lattice mismatch, bonding between the atoms of the adjacent layers are weak, and the adjacent layers could crack, separate, or have a large number of crystalline defects. Therefore, the nucleation layer 18 operates to correct the lattice mismatch between the AlN sub-buffer layer 20 and the substrate 12 by creating an interface between the crystalline structure of the substrate 12 and the crystalline structure of the AlN sub-buffer 20.

[0018] After depositing the nucleation layer 18, the AlN sub-buffer layer 20 is deposited on the nucleation layer 18. Once the AlN sub-buffer layer 20 is deposited on the nucleation layer 18, the GaN buffer layer 22 is deposited on the AlN sub-buffer layer 20, and the AlGaN Schottky layer 24 is deposited on the GaN buffer layer 22. A two dimensional electron gas (2-DEG) conduction channel, which is a thin, high mobility channel, confines carriers to an interface region illustrated by a dashed line between the GaN buffer layer 22 and the AlGaN Schottky layer 24. The GaN termination layer 26 is deposited on the AlGaN Schottky layer 24 and serves as a reproducible termination layer.

[0019] The PSN passivation layer 16 is deposited on the GaN termination layer 26 after the deposition of the structural epitaxial layers 14 on the substrate 12 while the GaN structure 10 is still in the growth chamber. Preferably, the PSN passivation layer 16 is deposited on the structural epitaxial layer 14 immediately following the deposition of the structural epitaxial layers 14 on the substrate 12. As discussed above, the PSN passivation of the GaN structure 10 before removing the GaN structure 10 from the growth chamber prevents exposure of the surface of the structural epitaxial layers 14 to air before passivation. In addition, for embodiments that

do not include the GaN termination layer 26, the PSN passivation layer 16 prevents oxidation of the AlGaN Schottky layer 24 when the GaN structure 10 is exposed to air.

[0020] Figure 2 illustrates a high electron mobility transistor (HEMT) 28 fabricated using the GaN structure 10 (Figure 1). The PSN passivation layer 16 passivates the surface traps on the surface of the structural epitaxial layers 14 in regions between a source contact 30 and a gate contact 32 and between the gate contact 32 and a drain contact 34. The PSN passivation layer 16 essentially eliminates degradation of operation of the HEMT 28 due to phenomena associated with the surface traps, such as radio frequency (RF) dispersion and current collapse. For example, current collapsing occurs when a large bias voltage is applied between the source contact 30 and the drain contact 34.

[0021] As discussed above, the optional GaN termination layer 26 is a reproducible termination layer and is not necessary for the present invention. In the preferred embodiment, the GaN termination layer 26 is approximately 1-2 nanometers thick. Therefore, electrons can easily tunnel through the GaN termination layer 26. As a result, the GaN termination layer 26 does not increase the Schottky barrier height between the gate contact 32 and the AlGaN Schottky layer 24, where the Schottky barrier height defines a potential energy barrier encountered by electrons at the interface of the gate contact 32 and the AlGaN Schottky layer 24. Further, the GaN termination layer 26 does not affect the formation of the source and drain contacts 30 and 34.

[0022] The AlN sub-buffer layer 20 improves the performance of the HEMT 28 by preventing injection of electrons into the nucleation layer 18 and the substrate 12 during high-power operation of the HEMT 28. As a result, a source-drain breakdown voltage for the HEMT 28 improves from approximately 20 volts to more than 100 volts. Therefore, the HEMT 28 may be used in a high power GaN amplifier (not shown). As discussed above, the AlN sub-buffer layer 20 is optional and is not necessary for the present invention.

[0023] During fabrication of the HEMT 28, the PSN passivation layer 16 is etched in a first region to connect the source contact 30, in a second region to connect the gate contact 32, and in a third region to connect the drain contact

34 to the GaN termination layer 26. In an alternative embodiment that does not include the GaN termination layer 26, the contacts 30, 32, and 34 are formed on the AlGaN Schottky layer 24. The gate contact 32 is a metallic material such as but not limited to nickel gold. The source and drain contacts 30 and 34, respectively, are ohmic contacts. Further, the source and drain contacts 30 and 34, respectively, are each a metallic material such as but not limited to titanium gold, titanium aluminum, or titanium.

[0024] For the gate contact 32, the PSN passivation layer 16 is preferably etched using a wet chemical etch, in order to avoid plasma-induced surface damage that would adversely affect operation of the gate contact 32 and the HEMT 28. Alternatively, the gate opening can also be made by dry etching methods with a fluorine or chlorine based etch. For the source contact 30 and the drain contact 34, the PSN passivation layer 16 may be etched using either wet or dry chemical etching, such as but not limited to fluorine-based reactive ion etching. Further, plasma induced surface damage may improve ohmic contact of the source contact 30 and the drain contact 34 to the structural epitaxial layers 14.

[0025] Figure 3 illustrates an embodiment of the present invention that is similar to the HEMT 28 in Figure 2, and in particular Figure 3 illustrates a metal-insulator-semiconductor field effect transistor (MISFET) 36. In this embodiment, the MISFET 36 is fabricated by forming the gate contact 32 on the PSN passivation layer 16 and the source and drain contacts 30 and 34 on the GaN termination layer 26. The details of the MISFET 36 with respect to the present invention are similar to the details of the HEMT 28 in Figure 2. In general, the PSN passivation layer 16 serves to passivate the surface traps on the surface of the structural epitaxial layers 14, thereby preventing device degradation due to phenomena associated with the surface traps such as but not limited to RF dispersion and current collapse.

[0026] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present invention. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.